Isfahan University of Technology
Electrical & Computer Department

Special Topic in Computer Network

System Packet Interface

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Agenda

- Introduction
- What is OIF
- OIF Electrical Interfaces
- What is SPI
  - the physical implementation of the bus
  - the signaling protocol used to communicate data
  - the data structures used to transmit data over the interface
- Overview of other version SPI

Introduction

- **What is interface**
- **Benefits of Specified Interfaces**
  - **Partition complex problem into solvable pieces**
  - **Consistency of interfaces among vendors**
  - **Reduce time to market**
  - **Increase integration success**
- **Network interface**
  - **Software interface**
  - **Hardware interface**

What is OIF

- OIF is acronym of Optical Internetworking Forum
- Launched in April of 1998 with an objective to foster development of low-cost and scaleable internet using optical technologies
- The only industry group bringing together professionals from the data and optical communities
- Open forum: 250+ member companies
  - international
  - carriers
  - component and systems vendors
  - testing and software companies
- Mission: To foster the development and deployment of interoperable products and services for data switching and routing using optical networking technologies

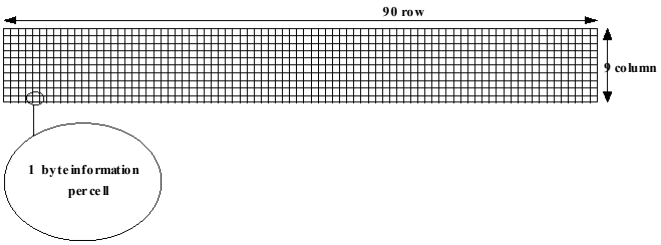
OIF structure

- Carrier
  Requirements and applications
- Architecture
  Services, network requirements and architectures
- Signaling
  Protocols for automatic management of optical connections
- OAM&P (Operations, Administration, Maintenance and Provisioning)
  Network management
- *Physical and Link Layer (PLL)* ⇦
  Equipment and subsystem module interfaces
- Interoperability
  Interoperability testing

SONET

- (PLL) Working Group within the OIF has defined electrical interfaces at two different points within a Synchronous Optical NETwork/ Synchronous Digital Hierarchy (SONET/SDH) based communication system.
- Synchronous Optical NETwork **(**SONET) is a standard for optical communication transport.
- SONET define Optical Carrier (OC) levels.
- The basic unit of transport defined by SONET is the STS-1 frame. This STS-1 frame is organized as a matrix of nine rows of 90 bytes each, for a total of 810 bytes per frame.
- Bytes are transmitted one at a time, from left to right starting with row one.

SONET



- As is the case with other digital hierarchies, 8000 SONET frames are transmitted per second—one complete frame of 810 bytes is transmitted every 125 microseconds. The 51.84 Mbps transmission rate of STS-1 (OC-1) is achieved as follows:
- 8000 frames/second * 810 bytes/frame * 8 bits/byte = 51840000 bits/second = 51.84 Mbps

SONET

- transmission rate of OC-1= 51.84 Mbps
- So for OC-N transmission rate =n* 51.84 Mbps

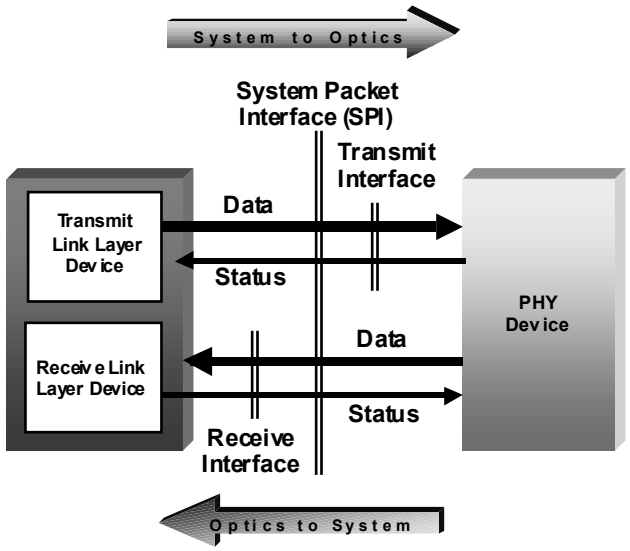
Optical carrier level	Transmission rate (Mbps)
OC-48	2.48832 Mbps
OC-192	9953.28~=10Gbps
OC-768	39813.12~=40Gbps

System Packet Interface

- SPI is an interface for packet and cell transfer between a physical layer (PHY) device and a link layer device.
- As shown in the following table, four electrical interface Implementation Agreements have been published by the OIF during the last years.

Interface	Year
SPI-3	1999
SPI-4 P1	2000
SPI-4 P2	2000
SPI-5	2002

System Packet Interface (SPI-n)



SPI-4 P2

- Now SPI-4 P2 is selected to describe completely, other SPI-n are can be understand after. In the next section describe different between them.

- SPI-4 P2 is interface for the interconnection of Physical Layer (PHY) devices to Link Layer devices for 10 Gb/s aggregate bandwidth applications by means of a higher-speed interface than defined in SPI-4 Phase 1. This Phase 2 specification will be referred to hereon for convenience in this section as the SPI-4 interface.

- SPI-4 is an interface for packet and cell transfer between a physical layer (PHY) device and a link layer device, for aggregate bandwidths of OC-192 ATM and Packet over SONET/SDH (POS), as well as 10 Gb/s Ethernet applications.

SPI-4 P2

- overview of SPI-4 interface:
- Point-to-point connection (i.e., between single PHY and single Link Layer device).
- Support for 256 ports (suitable for STS-1 granularity in SONET/SDH applications (192 ports) and Fast Ethernet granularity in Ethernet applications (100 ports)).

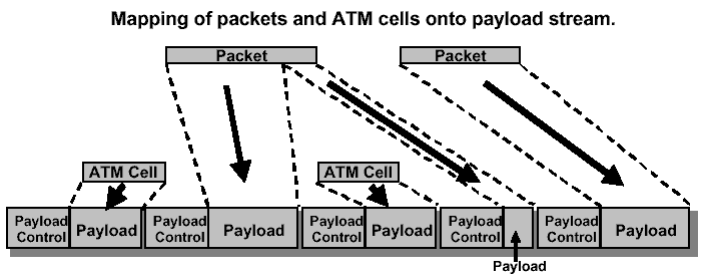
- Transmit / Receive Data Path:
  - 16 bits wide.
  - In-band port address, start/end-of-packet indication, error-control code.
  - LVDS I/O (IEEE 1596.3 – 1996 [1], ANSI/TIA/EIA-644-1995 [2]).
  - 622 Mb/s minimum data rate per line.
  - Source-synchronous double-edge clocking, 311 MHz minimum.

SPI-4 P2

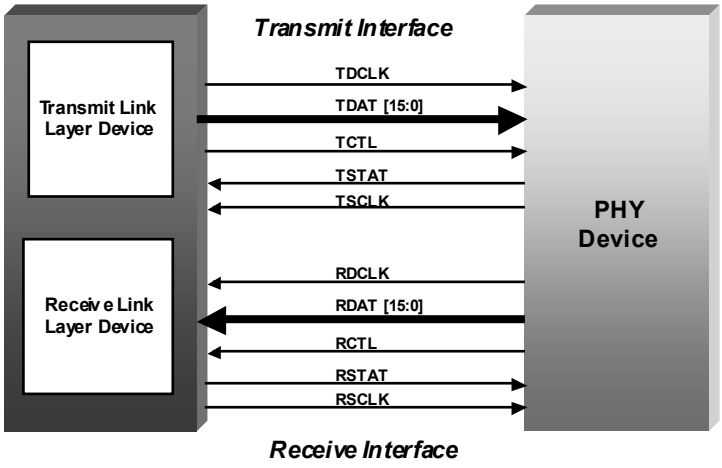
- Transmit / Receive FIFO Status Interface:
  - LVTTL I/O or optional LVDS I/O (IEEE 1596.3 – 1996 [1],ANSI/TIA/EIA-644-1995 [2]).
  - Maximum 1/4 data path clock rate for LVTTL I/O, data path clock rate (double-edge clocking) for LVDS I/O.
  - 2-bit parallel FIFO status indication.
  - In-band Start-of-FIFO Status signal.
  - Source-synchronous clocking.

SPI-4 P2

- How data is transferred?



SPI-4 P2 (signals)



SPI-4 P2 (signals)

- **TDCLK (Transmit Data Clock)**
  TDCLK is a clock associated with TDAT and TCTL. TDCLK provides the datapath source-synchronous double-edge clocking with a minimum frequency of 311 MHz. Data and control lines are driven off the rising and falling edges of the clock. TDCLK is sourced by the MAC to the PHY.
- **TDAT[15:0] Transmit Data**
  TDAT is a 16-bit bus used to carry payload data and in-band control words from the Link Layer to the PHY device. A control word is present on TDAT when TCTL is high. The minimum data rate for TDAT is 622 Mb/s.
- **TCTL (Transmit Control)**
  TCTL is high when a control word is present on TDAT, otherwise it is low. TCTL is sourced by the MAC to the PHY.
- **TSCLK (Transmit Status Clock)**
  TSCLK is a clock associated with TSTAT providing source-synchronous clocking. For LVTTL I/O a maximum clockrate restraint is ¼ that of the data path clock rate. LVDS I/O allows a maximum of that equal to the data path clock (double-edge clocking).

SPI-4 P2 (signals)

- **TSTAT[1:0] (Transmit FIFO Status)**

  TSTAT is a 2-bit bus used to carry round-robin FIFO status information, along with associated error detection and framing. The maximum data rate for TSTAT is dependent on the I/O type, either LVDS or LVTTL, and is limited to its respective TSCLK restraints. TSTAT is sourced by the PHY to the MAC. The FIFO status formats are:

  TSSTAT[1:0] = "11" Reserved for framing or to indicate a disabled status link.

  TSSTAT[1:0] = "10" SATISFIED

  TSSTAT[1:0] = "01" HUNGRY

  TSSTAT[1:0] = "00" STARVING

SPI-4 P2 (signals)

- **RDCLK (Receive Data Clock)**

  RDCLK is a clock associated with RDAT and RCTL. RDCLK provides the atapath source-synchronous double-edge clocking with a minimum frequency of 311 MHz. Data and control lines are driven off the rising and falling edges of the clock. RDCLK is sourced by the PHY to the MAC.

- **RDAT[15:0] (Receive Data)**

  RDAT is a 16-bit bus which carries payload data and in-band control from the PHY to the Link Layer device. A control word is present on RDAT when RCTL is high. The minimum data rate for RDAT is 622 Mb/s.

- **RCTL (Receive Control)**

  RCTL is high when a control word is present on RDAT, otherwise it is low. RCTL is sourced by the PHY to the MAC.

SPI-4 P2 (signals)

- **RSCLK (Receive Status Clock)**

  RSCLK is a clock associated with RSTAT providing source-synchronous clocking. RSCLK is sourced by the Mac to the PHY. LVDS I/O allows a maximum of that equal to the data path clock (double-edge clocking).

- **RSTAT[1:0] (Receive FIFO Status)**

  RSTAT is a 2-bit bus used to carry round-robin FIFO status information, along with associated error detection and framing. The maximum data rate for RSTAT is dependent on the I/O type, either LVDS or LVTTL, and is limited to its respective RSCLK restraints. RSTAT is sourced by the Mac to the PHY. The FIFO status formats are:

  TSSTAT[1:0] = "11" Reserved for framing or to indicate a disabled status link.

  TSSTAT[1:0] = "10" SATISFIED

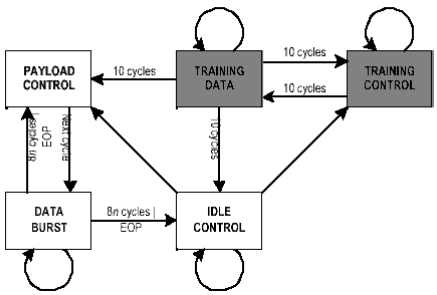
  TSSTAT[1:0] = "01" HUNGRY

  TSSTAT[1:0] = "00" STARVING

SPI-4 P2 (Data Path)

- The maximum configured payload data transfer size must be a multiple of 16 bytes. Control words are inserted only between burst transfers,
- Following state diagram shows cycle-by-cycle behavior of the data path for valid state transitions.The states correspond to the type of words transferred on the data path.

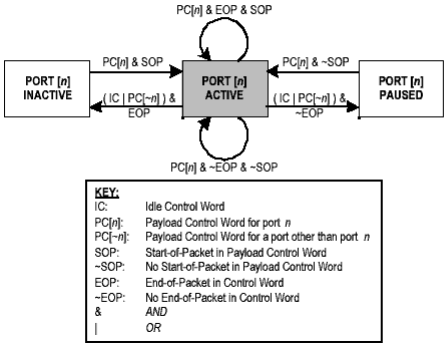
Data Path State Diagram.



SPI-4 P2 (control word)

- shows per-port state transitions at control word boundaries. At any given time, a given port may be active (sending data), paused (not sending data, but pending the completion of an outstanding packet), or inactive (not sending data, no outstanding packet).

Per-Port State Diagram with Transitions at Control Words.



SPI-4 P2 (control word)

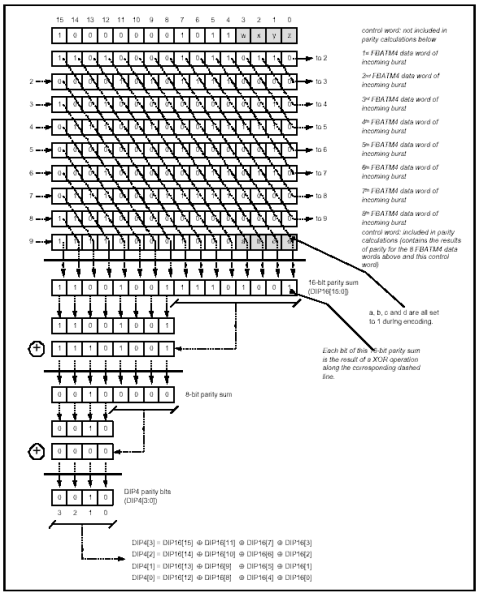
Bit Position	Label	Description
15	Type	Control Word Type. Set to either of the following values: 1: payload control word (payload transfer will immediately follow the control word). 0: idle or training control word (otherwise).
14:13	EOPS	End-of-Packet (EOP) Status. Set to the following values below according to the status of the immediately preceding payload transfer. 0 0: Not an EOP. 0 1: EOP Abort (application-specific error condition). 1 0: EOP Normal termination, 2 bytes valid. 1 1: EOP Normal termination, 1 byte valid. EOPS is valid in the first control word following a burst transfer. It is ignored and set to "0 0" otherwise.

SPI-4 P2 (control word)

12	SOP	Start-of-Packet. Set to 1 if the payload transfer immediately following the control word corresponds to the start of a packet. Set to 0 otherwise. Set to 0 in all idle and training control words.
11:4	ADR	Port Address. 8-bit port address of the payload data transfer immediately following the control word. None of the addresses are reserved (all are available for payload transfer). Set to all zeroes in all idle control words. Set to all ones in all training control words.
3:0	DIP-4	4-bit Diagonal Interleaved Parity. 4-bit odd parity computed over the current control word and the immediately preceding data words (if any) following the last control word.

SPI-4 P2

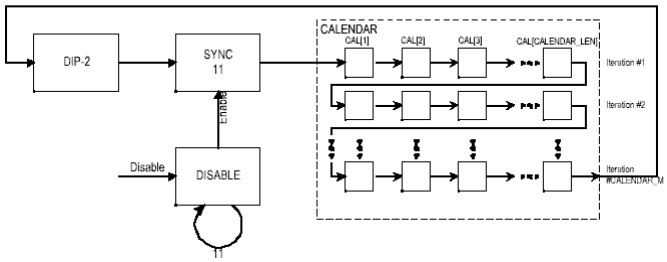
Example of DIP-4 Encoding (Odd Parity).



SPI-4 P2 (FIFO)

- The sequence of ports at a FIFO status channel is defined in a data structure called CALENDAR, where CALENDAR[i], i = 1,…,CALENDAR_LEN, refers to the ith port in the repeating sequence.

FIFO Status State Diagram (Sending Side)



SPI-4 P2 (FIFO)

- **Examples:**
- 1. Single OC-192 or 10 Gb/s Ethernet port: CALENDAR_LEN = 1,CALENDAR[1] = 1.
- 2. Four OC-48 ports: CALENDAR_LEN = 4, CALENDAR[i] = 1, 2, 3, 4.

SPI-4 P2

The importance of phase alignment has grown as source-synchronous interface protocols reach data rates close to 1 Gbps. At these rates, the slightest mismatch between clocks and their associated data signals due to board-level phenomena like skew and jitter can result in data transfer errors. DPA (Dynamic Phase Alignment) reduces the impact of these effects by repeatedly comparing incoming data with the system clock and continuously aligning the clock to match the data bits. Many interface standards organizations have incorporated DPA recommendations and requirements into their interfaces, including the Optical Internetworking Forum (OIF) with the System Packet Interface Level 4 (SPI-4) Phase 2 standard.

SPI-4 P2 (Higher Bandwidth Operation)

- Applications which require higher FIFO Status Channel bandwidths than feasible with LVTTL I/O, may optionally use LVDS I/O instead. If LVDS I/O is used, double-edge clocking is used on TSCLK and RSCLK, running at the same rate as the corresponding data path rate. The framing structure and operation of TSTAT[1:0] and RSTAT[1:0] remain unchanged.
- A training sequence is scheduled to be sent at least once every preconfigured bounded interval (FIFO_MAX_T) on both the transmit and receive FIFO Status interfaces.

SPI-4 P2

- **Training Sequence for Data Path Deskew**
- **A training sequence is scheduled to be sent at least once every preconfigured bounded interval (DATA_MAX_T) on both the transmit and receive data paths.**

Other SPI version

- SPI 3
  - Allowance for an 8-bit bus or a 32-bit bus interface
  - OC-3
  - No error checking
- SPI 4-P1
  - 64-bit single ended HSTL Class 1 I/O at 200 MHz supporting transfer rates of 12.8 Gb/s.
- SPI 5
  - Support for 256 ports with address extension to 2^{144} ports.
  - 2.488 Gb/s minimum data rate per line on data path
  - USE OC-768(40Gbps)

SPI-4 P2 (Start-Up Parameters)

- **Specified these parameters**
  - **CALENDAR_LEN**
  - **CALENDAR_M**
  - **MaxBurst1**
  - **MaxBurst2**
  - **FIFO_MAX_T**
  - **FIFO_MAX_T**
  - **a(**Number of repetitions of the data training sequence that must be scheduled every)

Glossary

- PLL - Physical and Link Layer Working Group
- SPI - System Packet Interface
- OC – Optical carrier
- SONET - Synchronous Optical NETwork
- OIF - Optical Internetworking Forum
- OAM&P - Operations Administration, Maintenance, & Provisioning Working Group
- PHY- physical layer
- DIP - Diagonal Interleaved Parity

References

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